Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) ~~In a system having a received PN clock signal, a~~ A method for providing a synchronized system clock signal having reduced jitter in a system having a received PN clock signal, said synchronized system clock signal being synchronized with said received PN clock signal, comprising the steps of:

providing a stable high frequency reference signal;

dividing said high frequency reference signal ~~to provide~~ which allows a system clock signal ~~having~~ to have one of a plurality of system clock phases; ~~and~~

recovering said received PN clock signal by providing PN phase adjustments of said received PN clock signal;

generating a tracking control signal in response to said PN phase adjustments for adjusting said system clock phase to one of the plurality of available phases; and

~~adjustably selecting a~~ adjusting said system clock phase ~~of said plurality of system clock phases~~ in accordance with the ~~received PN signal in order~~ tracking control signal to provide said synchronized system clock signal.

2. (Currently Amended) The method of claim 1, wherein said tracking control signal indicates the amount of the adjustment to make to said system clock phase, wherein said adjustment can be in the positive or negative direction ~~further comprising the step of recovering said received PN clock signal by providing PN phase adjustments of said received PN clock signal~~.

3. (Currently Amended) The method of claim 1, wherein ~~further comprising the step of providing a~~ the tracking control signal indicates the number of adjustments to make to said system clock phase, wherein said adjustment can be in the positive or negative direction ~~in accordance with said PN phase adjustments~~.

4. (Cancelled)

5. (Original) The method of claim 1 further comprising the step of multiplying said high frequency reference signal prior to dividing said high frequency reference signal.

6. (Original) The method of claim 1 wherein said high frequency signal is provided using a temperature compensated crystal oscillator.

7. (Currently Amended) A communication system for providing a synchronized system clock signal having reduced jitter, said system having a received pseudorandom number (PN) clock signal, said synchronized system clock signal being synchronized with said PN clock signal, the system comprising:

circuitry configured to provide ~~means for providing~~ a stable high frequency reference signal;

a divider to divide ~~means for dividing~~ said high frequency reference signal ~~to provide~~ which allows a system clock signal ~~having~~ to have one of a plurality of system clock phases; ~~and~~

circuity configured to recover said received PN clock signal by providing PN phase adjustments of said received PN clock signal;

circuitry configured to generate a phase adjustment signal for adjusting a system clock phase to one of the plurality of available phases ; and

circuitry configured to ~~means for adjustably selecting a~~ adjust said system clock phase ~~of said plurality of system clock phases~~ in accordance with the ~~received PN signal in order~~ phase adjustment signal to provide said synchronized system clock signal.

8. (New) The system of claim 1 wherein said tracking control signal indicates the amount of the adjustment to make to said system clock phase, wherein

said adjustment can be in the positive or negative direction

9. (New) The system of claim 1, wherein the tracking control signal indicates the number of adjustments to make to said system clock phase, wherein said adjustment can be in the positive or negative direction.